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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,889	07/23/2003	Robert C. Klein JR.	126709.101	8888

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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,889	KLEIN, ROBERT C.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 8, 10-17, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kolchinsky (USPN 5,301,344).

4. As per Claim 1, Kolchinsky teaches: A reconfigurable processor for processing digital logic functions (Column 1, Lines 51-52), comprising:

a microcontroller (Column 4, Line 11, the "computer 10"); and

a plurality of processing elements (Column 1, Lines 57-61 and Column 2, Lines 33-34),

wherein the plurality of processing elements are arranged in one or more pipeline stages each comprising one or more processing elements (Column 1, Lines 63-66), and

wherein the microcontroller executes a program comprising:

configuring the plurality of processing elements by sending configuration information to the plurality of processing elements (Column 3, Lines 23-45),

determining whether data has been processed by the one or more processing elements of a pipeline stage (Column 4, Lines 10-17, the computer determines the opcode, and only afterwards, places it in the instruction operational code register), and

if data has been processed by the one or more processing elements of the pipeline stage, reconfiguring at least one of the one or more processing elements of a pipeline stage to define a subsequent pipeline stage (Column 4, Lines 17-39. After being processed by the computer and put in the register, the next stage's address generator file and arithmetic unit hardware is reconfigured (defined) for that instruction).

5. As per Claim 2, Kolchinsky teaches: The processor of claim 1 further comprising one or more decoders connected to the microcontroller, wherein each decoder is connected to one or more of the plurality of processing elements (Column 4, Lines 17-19, also see Figure 2).

6. As per Claim 3, Kolchinsky teaches: The processor of claim 2 further comprising one or more global interconnection busses used to connect the plurality of processing elements to the one or more decoders (Column 3, Lines 45-48).

7. As per Claim 4, Kolchinsky teaches: The processor of claim 2 wherein reconfiguring the plurality of processing elements is performed via the one or more decoders (Column 4, Lines 17-23).

8. As per Claim 5, Kolchinsky teaches: The processor of claim 1 further comprising a plurality of local interconnection busses (Column 3, Lines 45-48).

9. As per Claim 6, Kolchinsky teaches: The processor of claim 5 wherein each processing element is connected to one or more other processing elements by one or more of the local interconnection busses (Column 3, Lines 45-48).

10. As per Claim 8, Kolchinsky teaches: The processor of claim 1 wherein the microcontroller is in communication with a memory, and the program is stored in the memory (Column 4, Lines 3-8, the hard disk).

11. As per Claim 10, Kolchinsky teaches: A method of dynamically reconfiguring a pipelined instruction set processor comprising:

configuring a plurality of pipeline stages by a microcontroller (Column 3, Lines 23-45), wherein each pipeline stage includes one or more processing elements (Column 1, Lines 57-61 and Column 2, Lines 33-34, the programmable logic blocks/programmable gate arrays);

processing data through one or more of the plurality of pipeline stages (Column 4, Lines 22-23);

reconfiguring, by the microcontroller, at least one of the one or more pipelined stages to define at least one subsequent pipeline stage (Column 4, Lines 17-39. After being processed by the computer and put in the register, the next stage's address

generator file and arithmetic unit hardware is reconfigured (defined) for that instruction); and

routing processed data through the at least one reconfigured pipeline stage (Column 4, Lines 2-39, the stage is configured then executed).

12. As per Claim 11, Kolchinsky teaches: The method of claim 10 wherein the reconfiguring step is performed while the processed data is further processed by the plurality of pipelined stages (Column 4, Lines 19-39. Also see Figure 2. While data is being processed and reconfigured in steps 54 and 56 for the address generator file, data is simultaneously being processed and reconfigured in steps 60 and 62 for the arithmetic unit hardware).

13. As per Claim 12, Kolchinsky teaches: A reconfigurable processor for processing digital logic functions, comprising:

an on-chip microcontroller (Column 4, Line 11, the "computer 10"); and

a plurality of processing elements (Column 1, Lines 57-61 and Column 2, Lines 33-34, the programmable logic blocks/programmable gate arrays),

wherein the plurality of processing elements are arranged in one or more pipeline stages each comprising one or more processing elements (Column 1, Lines 63-66), and

wherein the microcontroller executes a program comprising:

configuring the plurality of processing elements by sending configuration information to the plurality of processing elements (Column 3, Lines 23-45),

determining whether data has been processed by the one or more processing elements of a pipeline stage (Column 4, Lines 10-17, the computer determines the opcode, and only afterwards, places it in the instruction operational code register), and

if data has been processed by the one or more processing elements of the pipeline stage, reconfiguring at least one of the one or more processing elements of a pipeline stage to define a subsequent pipeline stage (Column 4, Lines 17-39. After being processed by the computer and put in the register, the next stage's address generator file and arithmetic unit hardware is reconfigured (defined) for that instruction).

14. As per Claim 13, Kolchinsky teaches: The processor of claim 12 further comprising one or more decoders connected to the microcontroller, wherein each decoder is connected to one or more of the plurality of processing elements (Column 4, Lines 17-19, also see Figure 2).

15. As per Claim 14, Kolchinsky teaches: The processor of claim 13 further comprising one or more global interconnection busses used to connect the plurality of processing elements to the one or more decoders (Column 3, Lines 45-48).

16. As per Claim 15, Kolchinsky teaches: The processor of claim 13 wherein configuring the plurality of processing elements is performed via the one or more decoders (Column 4, Lines 17-23).

17. As per Claim 16, Kolchinsky teaches: The processor of claim 12 further comprising a plurality of local interconnection busses (Column 3, Lines 45-48).

18. As per Claim 17, Kolchinsky teaches: The processor of claim 16 wherein each processing element is connected to one or more other processing elements by one or more of the local interconnection busses (Column 3, Lines 45-48).

19. As per Claim 19, Kolchinsky teaches: The processor of claim 12 wherein the microcontroller is in communication with a memory, and the program is stored in the memory (Column 4, Lines 3-8, the hard disk).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kolchinsky, in view of Birrittella et al. (USPN 5,737,628, herein Birrittella).

22. As per Claim 7, Kolchinsky teaches the processor of claim 6, but fails to teach: wherein the plurality of processing elements are interconnected in a toroidal interconnect structure.

Kolchinsky has taught an interconnect network between the processing elements (Column 3, Lines 45-48), but has not disclosed in what structure the elements are interconnected. Birrittella teaches that as the number of processing nodes in a system increase, a balance needs to be struck between interconnect dentist and communication latency, as direct connection between all nodes becomes impossible (Background of the invention). Birrittella teaches that a torus interconnection network has the advantages of speed of information transfers, and the ability to avoid bad communications links (Column 8, Lines 6-41). Given the need to interconnect the elements in some fashion, the advantages of a toroid routing network as disclosed by Birrittella would have motivated one of ordinary skill in the art at the time the invention was made to connect the processing elements of Kolchinsky's invention in a toroid, to take advantage of the speed and ability to bypass bad elements in the network.

23. As per Claim 18, Kolchinsky teaches the processor of claim 17, but fails to teach: wherein the plurality of processing elements are interconnected in a toroidal interconnect structure.

Kolchinsky has taught an interconnect network between the processing elements (Column 3, Lines 45-48), but has not disclosed in what structure the elements are interconnected. Birrittella teaches that as the number of processing nodes in a system increase, a balance needs to be struck between interconnect dentist and communication latency, as direct connection between all nodes becomes impossible (Background of the invention). Birrittella teaches that a torus interconnection network

has the advantages of speed of information transfers, and the ability to avoid bad communications links (Column 8, Lines 6-41). Given the need to interconnect the elements in some fashion, the advantages of a toroid routing network as disclosed by Birrittella would have motivated one of ordinary skill in the art at the time the invention was made to connect the processing elements of Kolchinsky's invention in a toroid, to take advantage of the speed and ability to bypass bad elements in the network.

24. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kolchinsky, in view of Agnew et al. (USPN 4,514,803, herein Agnew).

25. As per Claim 9, Kolchinsky teaches the processor of claim 1, but fails to teach: wherein the microcontroller is an off-chip device.

However, Agnew teaches that a microprocessor may off-chip, to take advantage of extendibility, flexibility, and lower development costs for off-chip code, for use in non-critical or time sensitive functions (Column 9, Lines 40-48). Given that advantage, it would have been obvious to one of ordinary skill in the art at the time the invention was made to consider moving the microcontroller off-chip, if the advantages of flexibility, extendibility, and lower development costs outweighed the disadvantage of slower speed. In addition, it has been established by *In re Japikse,* 181 F.2d 1019, 1023, 86 USPQ 70, 73 (CCPA 1950) that it would be within one of ordinary skill in the arts ability to move parts on or off the chip without changing the functionality.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

27. Terrill et al. (USPN 5,590,305) teaches a plurality of programmable logic devices which can be initialized, and then reconfigured dynamically either by themselves or by control from the user or software.

28. Abbott (USPN 6,006,321) teaches a programmable logic datapath for use in an FPGA, with a plurality of logic elements interconnected to each other, which each of which can be dynamically reconfigured on a cycle-by-cycle basis.

29. Donohoe (USPN 6,883,084) teaches a reconfigurable processor comprising a plurality of dynamically reconfigurable processing elements which comprise a pipeline.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert E Fennema
Examiner
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